A Novel Scalable Design of 2:4 Decoders for Power Estimation in Submicron Technology

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***Abstract*— In this paper, a scalable design of 2:4 Decoder has been designed to minimize power dissipation using 250nm, 180nm and 90nm CMOS technology. The proposed design has been simulated and analyzed in TANNER-13 EDA tool to make comparative study of power consumption at different technologies. The proposed scalable 2:4 Decoder using 90nm CMOS technology gives better results in terms of power consumption in 180nm and 250nm CMOS technologies. In this paper, also comparison of 2:4 decoders is done on the basis of average power consumption and maximum power consumption at constant voltages and at different nano-technologies.**

Keywords*— *Decoder, Power dissipation, scalable, CMOS, gates, etc.

I. INTRODUCTION

In present situation, power dissipation minimization is a major challenge in front of IC designers in the technology world. In microprocessors, digital signal processors (DSPs) and other applications design of low power circuit is major issue in digital system. The electronics world started with the vacuum tube which is then replaced by transistor and then SSI, MSI and now by VLSI chips. The power consumption has become an important consideration on the VLSI system design and microprocessor as the demand for the portable devices and embedded systems continuously increases. The development of microelectronic technology especially for those of monolithical IC's is able to produce interfaced circuit by combining all active and passive components in one chip. The on-chip caches can reduce the speed gap between the processor and main memory. These on-chip caches are usually implemented using memory cells. The write power is usually larger than the read power due to large power dissipation in driving the cell bit lines to full swing. The sum of the power consumption in decoders, bit lines, data lines, sense amplifier, and periphery circuits represents the active power consumption in memory. Decoder is an important part of the memory system which selects the particular cells to be write/read from array as shown in figure1.1. It accepts a value and decodes it this output corresponds to value of *n* inputs. It also is called many-to-one decoder, a decoder matrix or simply a decoder. Decoders are widely used in memory systems of computers, where they respond to the address code input from the central processor to activate the memory storage location specified by the address code. Decoders used whenever an output or a group of outputs is too activated only on the occurrence of specific combination of input levels. These input levels are often provided by the outputs of a counter or register. When the decoder inputs come from a counter that is being continually pulsed, the decoder outputs will be activated sequentially, and they can be used as timing or sequencing the signals to turn devices ON or OFF at specific times.

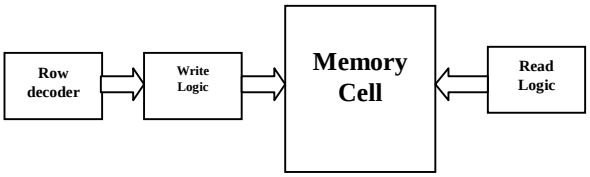

Figure1.1 Block Diagram of Memory System

II. OVERVIEW OF DECODERS

A decoder is a combinational device which does the reverse operation of an encoder. A decoder consists of n inputs and 2^n outputs. For example a 2:4 decoders as shown in figure 2.1 consist of n=2 inputs and 2^n=8 outputs. In digital logic design decoders have different forms such as BCD to seven segment decoders, all code converters, etc. Decoders also consists Enable pin, depends enable decoder is active otherwise it remained in off state. Logic design is guided by the requirements imposed on the implementation, such as performance and power. Decoder is important basic block in number of applications such as data multiplexing, 7 segment decoder and memory system design. Decoder circuit would be an AND gate because the output of an AND gate is "High" (1) only when all its inputs are "High" as shown in figure 2.2. Such output is called as "active High output". If instead of AND gate, the NAND gate is connected the output will be "Low" (0) only when all its inputs are "High". Such output is

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called as "active low output". A slightly more complex decoder would be the n-to-2n type binary decoders. These types of decoders are combinational circuits that convert binary information from 'n' coded inputs to a maximum of 2^n unique outputs. We can have 2-to-4 decoder, 3-to-8 decoder or 4-to-16 decoder.

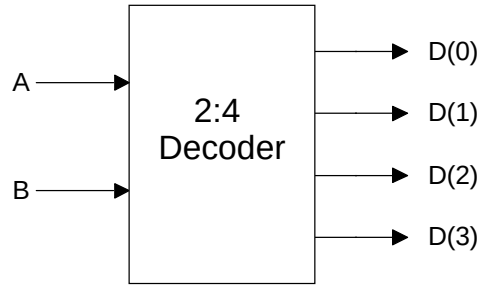


Figure2.1 Block Diagram of 2:4 Decoders

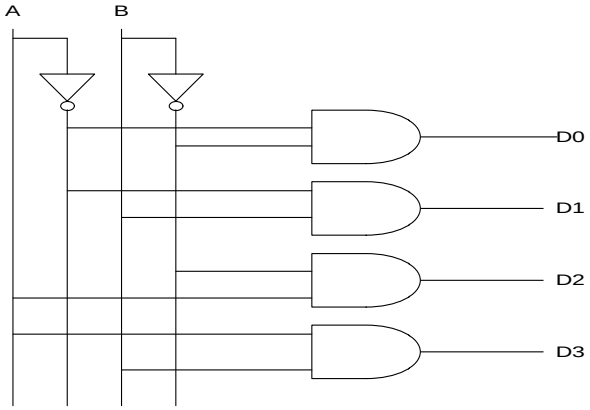


Figure 2.2 Circuit Diagram of 2:4 Decoders using Logic Gates

Figure 2.2 shows the circuit diagram of the decoder. In this diagram we realized the decoder expression using NOT gate and AND gate. The output is in term of the combination of the inputs. We have two inputs A and B and the outputs are D0, D1, D2, and D3. The Expression for the outputs is given as under:

D0 = A'B' ……(1)
D1 = A'B…….... (2)
D2 = AB'…….. (3)
D3 = AB ……(4)

Table 2.1: Truth Table of 2:4 Decoders "High Logic"

A	B	D3	D2	D1	D0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Table 2.1 Shows the Truth table of Decoder "Active High". In this table, according to the inputs the output is shown. The output D0 is high when both the input is low. The outputs D1 and D2 are high when one of the inputs is low. The output D3 is high when both the input is high.

According to figure 2.2 to design a 2:4 decoders 2- NOT gates and 4-AND gates are required. Such design of 2:4 decoders is called as "High Logic" designed of decoders. To implement the above design using CMOS, total twenty eight transistors are required.

Similarly, it is possible to design a decoder using NAND gate also. Such design of 2:4 decoders is called as "Low Logic" designed of decoders. Table 2.2 shows the Truth table of Decoder "Active Low". In this table, according to the inputs the output is shown. The output D0 is low when both the input is low. The outputs D1 and D2 are low when one of the inputs is low. The output D3 is low when both the input is high. To implement the NAND-decoders using CMOS, total numbers of transistors required are twenty.

Table 2.2: Truth Table of 2:4 Decoders "High Logic"

A	B	D3	D2	D1	D0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

III. PROPOSED SCALABLE 2:4 DECODER DESIGN TECHNIQUE

In conventional CMOS design, NAND and NOR gates are preferred to AND gate and OR gate, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2–4 decoder can be implemented with 2 inverters and 4 NOR gate Figure 3.1(a), whereas an inverting decoder requires 2 inverters and 4 NAND gates Figure3.1 (b), both yielding 20 transistors.

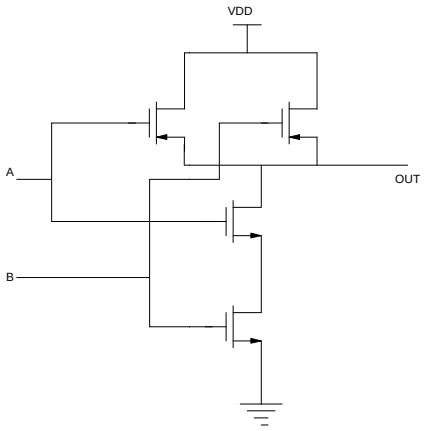


Figure 3.1(a) CMOS NAND gate circuit

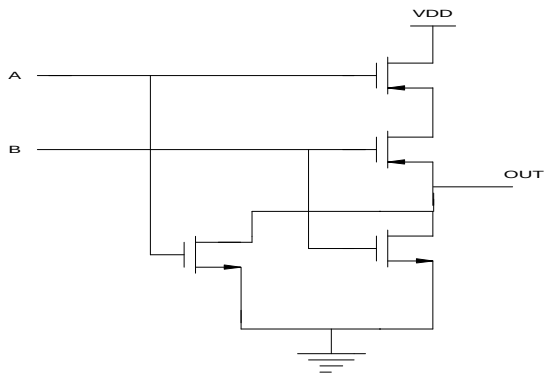


Figure 3.1(b) CMOS NOR gate circuit

Hence to implement 2:4 decoders total 20 transistors are required which is quite more and hence power dissipation also get increases. So in proposed design of 2:4 decoders we try to implement it with minimum number of transistor.

A) Schematic of 2:4 Decoders in 250nm

Scalable design of 2:4 decoders is implemented using only 10 transistors in which four transistors are used for 2 NOT gate and remaining 6 transistors form
a such combination whose output is very similar with traditional schematic of 2:4 decoder using 20 transistors. Scalable schematic of 2:4 decoders in 250nm is shown in figure 3.2.

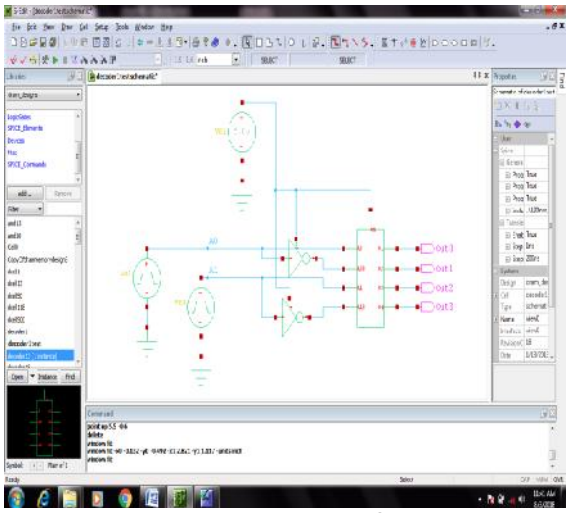


Figure 3.2 (a): Symbolic view of 2:4 Decoders

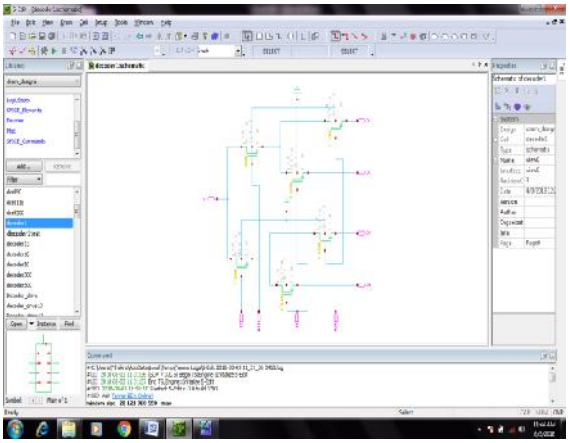


Figure 3.2 (b): Schematic view of 2:4 Decoders 250nm

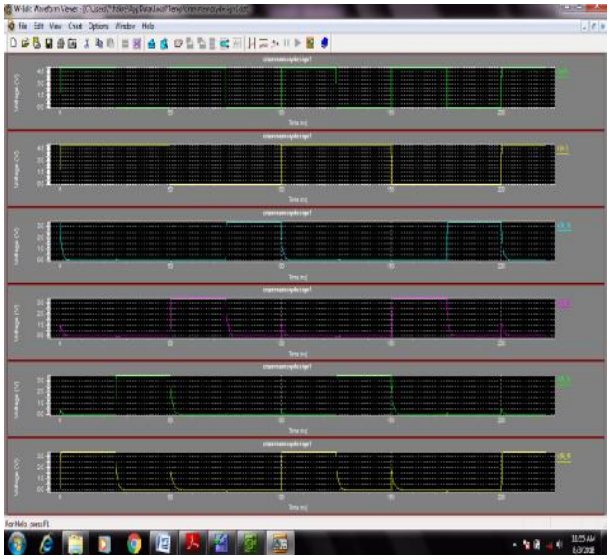


Figure 3.2(c): Output of 2:4 Decoders in 250nm

B) Schematic of 2:4 Decoders in 180nm

Scalable schematic of 2:4 decoders in 180nm is shown in figure 3.2(d).

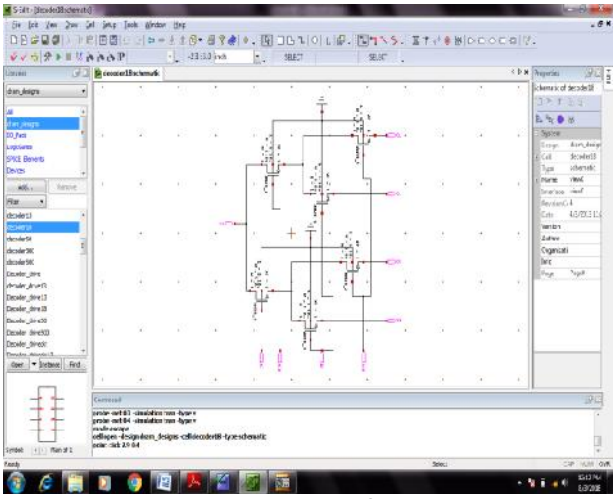


Figure 3.2 (d): Schematic view of 2:4 Decoders 180nm

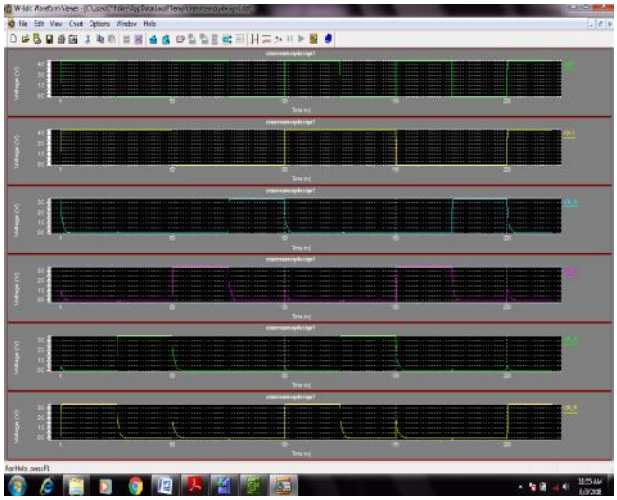


Figure 3.2(e): Output of 2:4 Decoders in 180nm

C) Schematic of 2:4 Decoders in 90nm

Scalable schematic of 2:4 decoders in 90nm is shown in figure 3.2(f).

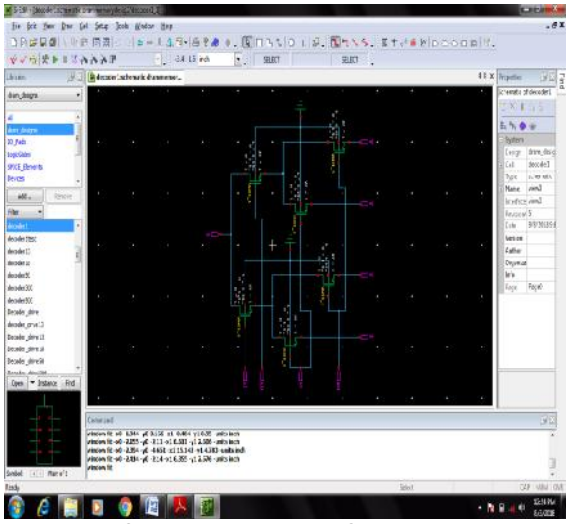


Figure 3.2 (f): Schematic view of 2:4 Decoders 90nm

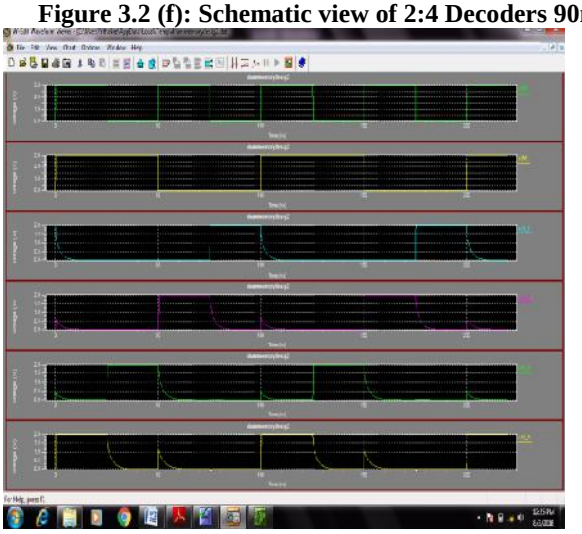


Figure 3.2 (g): Schematic view of 2:4 Decoders 90nm

IV. Result and Analysis

Comparison of proposed 2-to-4 Decoder is based on the performance parameters like power dissipation to achieve better performance using CMOS process by TANNER-13 in 250nm, 180nm and 90nm technology by T-spice command.

4.1 Power Dissipation in 250nm Technology

Power Results
vvs1 from time 1e-009 to 2e-007
Average power consumed -> 1.585512e-004 watts
Max power 1.375943e-002 at time 1.00557e-007
Min power 2.245069e-009 at time 1.04853e-007

4.2 Power Dissipation in 180nm Technology

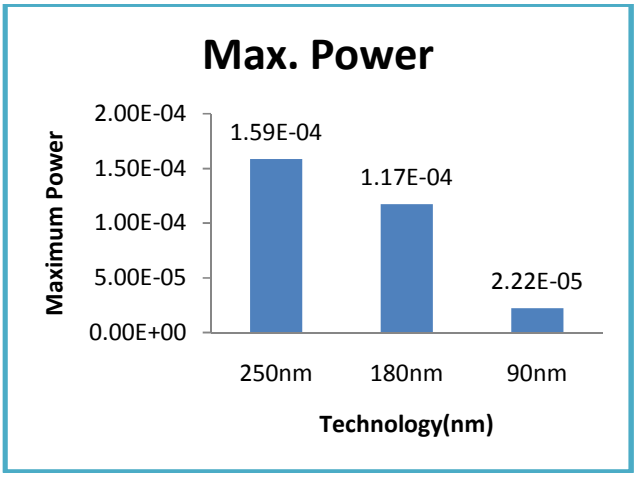
Power Results
vvs1 from time 1e-009 to 2e-007
Average power consumed -> 1.173591e-004 watts
Max power 1.166743e-002 at time 1.00682e-007
Min power 1.343535e-008 at time 1.61442e-007

4.3 Power Dissipation in 90nm Technology

Power Results
vvs1 from time 1e-009 to 2e-007
Average power consumed -> 2.224565e-005 watts
Max power 3.971014e-003 at time 1.00828e-007
Min power 2.948555e-006 at time 1.83586e-007

Table 4.1 Technology versus Power Dissipation

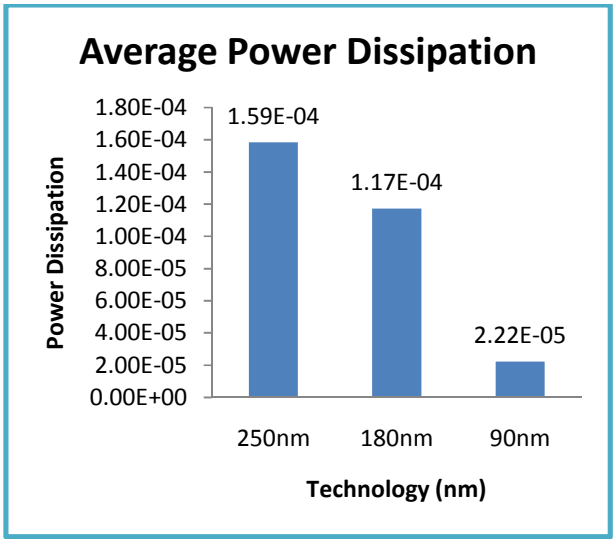
VDD	Technology	Max. Power
5v	250nm	1.375943e-002
5v	180nm	1.166743e-002
5v	90nm	3.971014e-003



Graph 4.1: Technology versus maximum power dissipation
According to above graph, as the technology changes from 250nm to 90nm the maximum power dissipation also gets decreases. At 90nm, 2:4 decoder shows lowest power dissipation.

Table 4.2 Technology versus Power Dissipation

VDD	Technology	Average Power
5v	250nm	1.59E-04
5v	180nm	1.17E-04
5v	90nm	2.22E-05



Graph 4.2: Technology versus maximum power dissipation

According to above graph, as the technology changes from 250nm to 90nm the average power dissipation also get decreases. At 90nm, 2:4 decoder shows lowest power dissipation.

V. Conclusion

The proposed 2:4 Decoder is designed and simulated using 250nm, 180nm and 90nm CMOS technologies. The performance parameter power is examined at 5V. Low power consumption is obtained using proposed logic for designed 2:4 Decoder. The power consumed by the circuit in 250nm, 180nm and 90nm CMOS technologies are 1.59E-04, 1.17E-04 and 2.22E-05 respectively. The novel scalable designed of 2:4 decoders required only 10 transistors as compared to traditional design of 2:4 decoders which required 20 transistors.

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