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Low Power Design Of Multiplier Using Feed Through Logic

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***Abstract*--**Continuous technologies climb and grow up frequency of operation of VLSI circuits leads to increase in power density which inflate thermal problem. Therefore design of low power VLSI circuit technique is a stimulating task without resign its performance. Multipliers play a vital role in today's digital signal processing and miscellaneous applications. Design aims high speed, low power utilization and hence less area or even combination of them in one multiplier thus making them suitable for different high speed, low power and compact VLSI implementation. High speed digital circuits FTL gives advantage of having lesser power utilization compared to any other logic families in literature. This paper represented a Modified FTL based on partial development concept. As the comparison table given is shown that FTL the 2-bit, 4-bit, 8-bit multiplier are 30%, 25% and 45% power are consumed and more efficient. The results confirmed that the multiplier using feed through logic is more efficient and low power consuming CMOS design. As per the result in tables, Modified FTL is suitable for high speed arithmetic, pipelining and filter circuit design over FTL.

***Keywords*--**Multiplier, Feedthrough logic (FTL) dynamic CMOS logic, low power adder, CMOS logic circuit.

I. INTRODUCTION:

Today multiplier plays a big role in digital signal processing and different applications. Such as microprocessor, DSP these are the high performance circuit etc. which are design by using addition and multiplication of two binary numbers and used for arithmetic operations. More than 70% operation in microprocessors and DSP algorithm is done on addition and multiplication [7]. So, these operation dominates the execution time. So, there is need of high speed multiplier. Nowadays there is demand of high speed processing and power consumptions device i.e. computers and signal processing application are increased [9].

In the multiplier the low power consumption is more important issue while designing. Inventors mainly focus on high speed and low power efficient circuit design. The intention of a good multiplier is high speed and low power consumption unit.

A new logic family is introduced known as feedthrough logic [5] which improves the performance of logic circuits basically for having long logic depth with reduced power dissipation [6].This logic works properly with domino concept for cascaded logic, differential style and multiple output with iterative networks has shown high design flexibility with the feature of partial evaluation of output before getting a valid input. This feature results in very fast evaluation of output in computational block [10].

Major advantage of feedthrough logic [5] is which does not require any additional circuits like keeper circuits for the reduction of leakage power and FTL can be cascaded without the use of inverters. In this paper a modified FTL based dynamic circuit is proposed for improved power reduction and better performance [10].

II. DIFFERENT MULTIPLIERS

An efficient multiplier should have following characteristics:-
Speed: - Multiplier should perform operation at high speed. **Area: -** A multiplier should occupies less number of slices and LUTs.**Accuracy: -** A good multiplier should give correct result.**Power: -** Multiplier should consume less power [8] [9].
There are four main steps for the multiplication:-

1. Multiplicand
2. Multiplier
3. Partial product generation
4. Final addition.

In the binary multiplication, the *n*-bit multiplicand is multiply with *m*-bit multiplier, *p* partial products are generated and product formed is *n*+*m* bits long. Here we are discussing three type of proposed multipliers using feed through logic and there results.

1. 2-bit multiplier with FTL
2. 4-bit multiplier with FTL
3. 8-bit multiplier with FTL.

2-BIT MULTIPLIER WITH FTL

Similar to the multiplication of decimal numbers, the same process for producing a product result of the two binary numbers is applicable in the binary multiplication also. The binary multiplication is easier as it contains only 0s and 1s. The following shows four fundamental rules for binary multiplication.

$0 \times 0 = 0$
$0 \times 1 = 0$
$1 \times 0 = 0$
$1 \times 1 = 1$

In this 2 –bit multiplier we use the feed through logic to design less power and efficient than normal multiplier CMOS circuit shown in Figure 1. For the multiplication of 2-bit by 2-bit we use full adder made from FTL to sum the partial products. Let we take B_1B_0 two binary bit as multiplicand and A_1A_0 as multiplier the product of both these is obtained as following procedure. Figure 1 shows the procedure of multiplication. The final addition is obtained while ANDing both the multiplicand and multiplier bit as we do in general multiplication. The $C_3C_2C_1C_0$ is the final addition obtained by adding the partial products. Figure 2 shows proposed 2-bit multiplier.

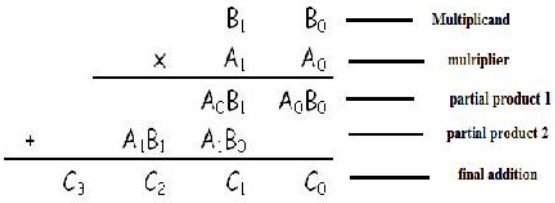


Figure1: Procedure of Multiplication

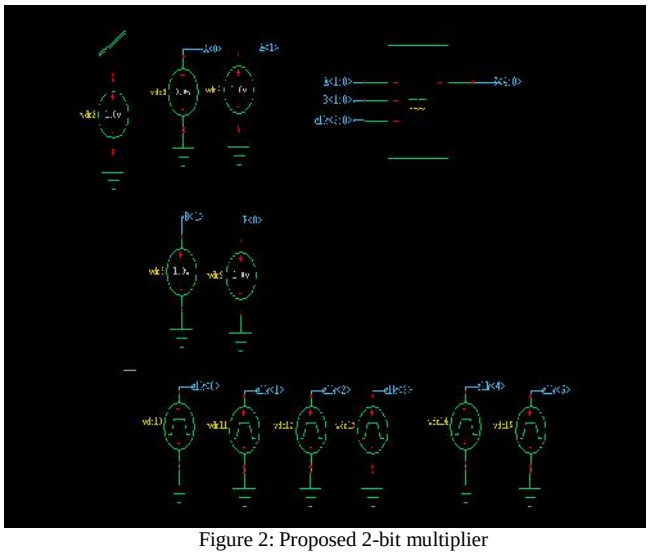
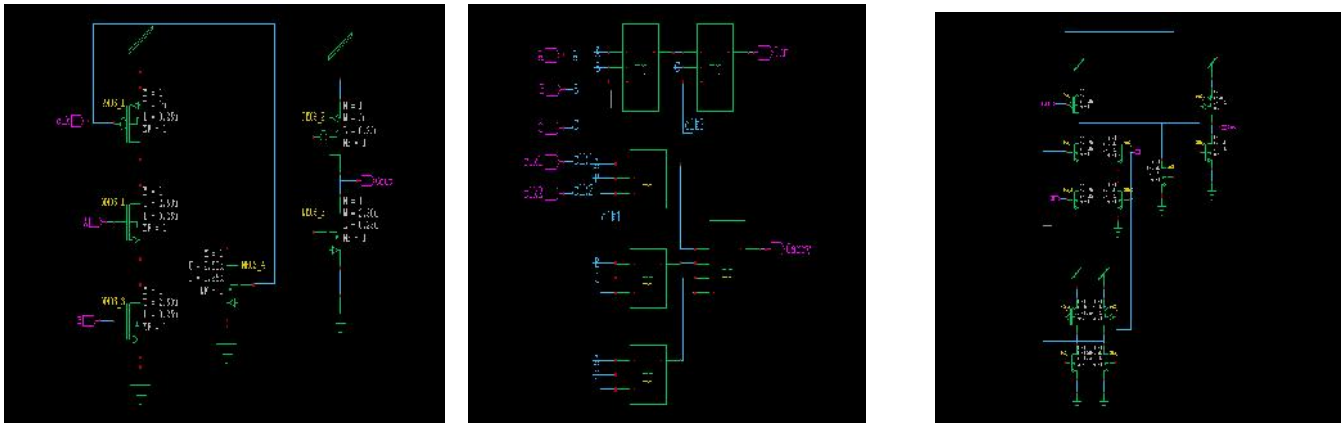
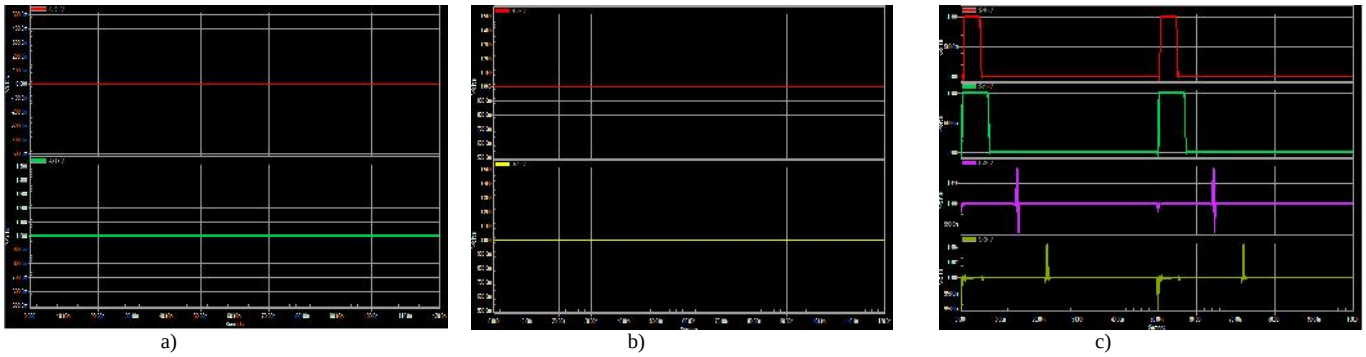


Figure 2: Proposed 2-bit multiplier



a) b) c)

Figure 3: a) AND gate using FTL b) Full adder symbolic representation c) Each Full adder is made from FTL.



a) b) c)

Figure 4: a) binary 2-bit A input b) binary 2-bit B input c) Output of multiplication

Let us consider A_1A_0=2 i.e. binary of 2 is 10 and B_1B_0=3 i.e. binary of 3 is 1. Then the output is C_1C_0= 6 i.e. binary of 6 is 101. The output waveform of these multiplication is shown below in figure 4.

4-BIT MULTIPLIER USING FTL

This 4bit multiplier is implemented by using three binary full adders along with AND gates. The below figure 5(a) shows the results of these multiplication. The first partial product is obtained by multiplication B_0 with $A_3A_2A_1A_0$, the second partial product is formed by multiplying B1 with $A_3A_2A_1A_0$ likewise for 3rd and 4th partial products. In this 4bit multiplier we use the multiplicand input A as 0100 i.e. binary of 4 and multiplier B as 0011 i.e. binary of 3 which gives after partial multiplication and then final addition 4*3=12 i.e. obtaining binary of 12 is obtained after simulation binary of 12 is 1100. Figure 5 (b) shows the symbol contain no of AND and Full Adder circuit. Figure 5(c) shows generalized CMOS design for 4-bit multiplier and figure 5(d), (e), (f) shows their basic waveform of each section.

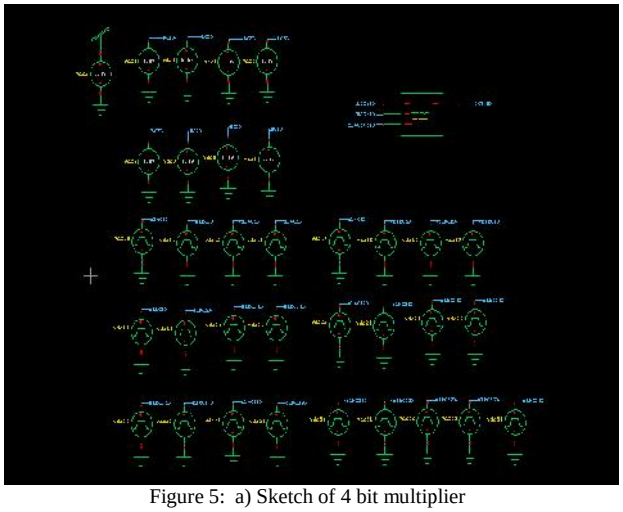
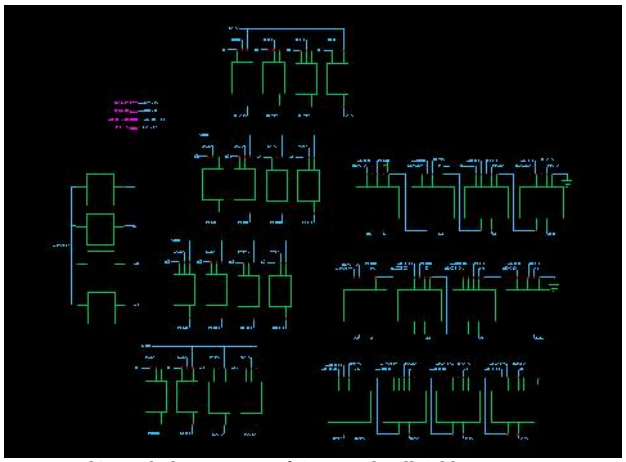
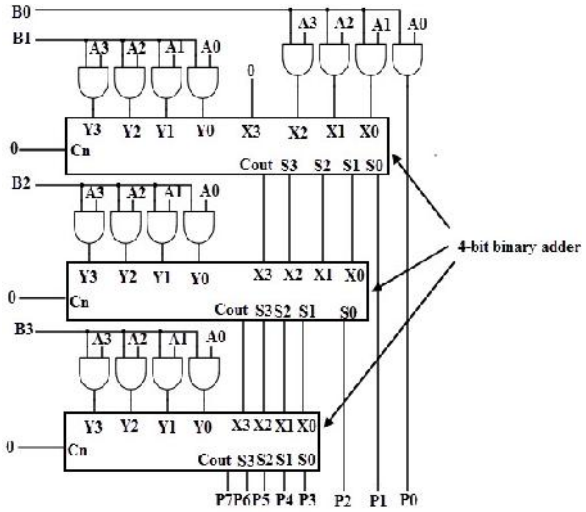


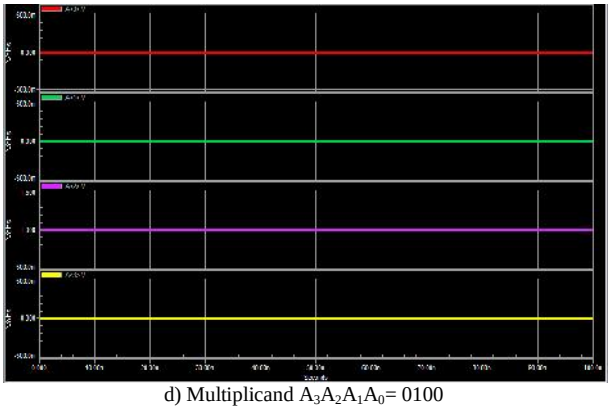
Figure 5: a) Sketch of 4 bit multiplier



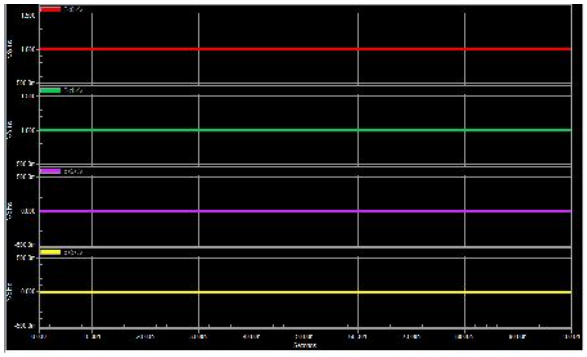
b) Symbol contain no of AND and Full Adder circuit



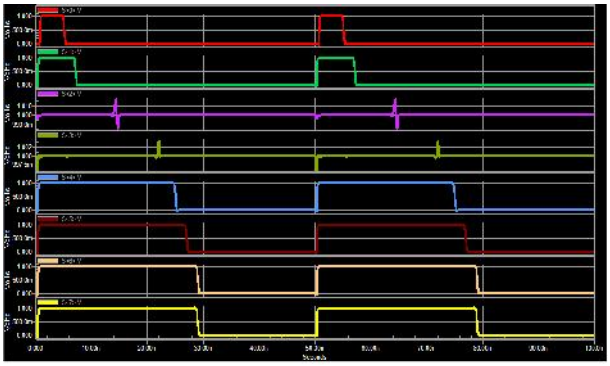
c) Generalized CMOS design for 4-bit multiplier



d) Multiplicand $A_3A_2A_1A_0$= 0100



e) Multiplier $B_3B_2B_1B_0$= 0011



f) Final result after multiplication

8 BIT MULTIPLIER USING FTL

Similarly in this multiplication there is also same condition apply that we use in 4-bit multiplication. All the FA and AND gate is design by using FTL. The optimum final result are shown in below figure. In the proposed 8-bit multiplier multiplicand A is in binary 00000100 and multiplier B is 00000011 is used. After giving partial products and final addition of the partial products the final result is shown in figure 6.

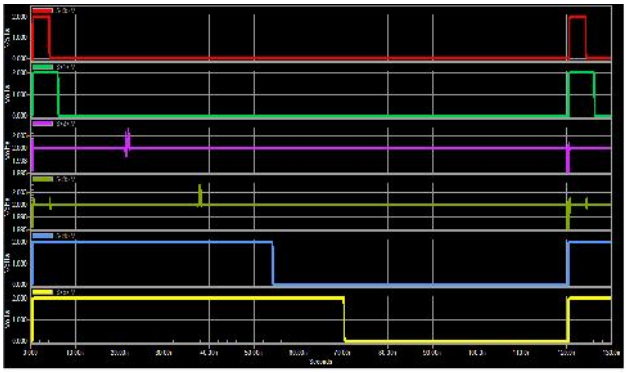


Figure 6: Final result of the multiplication

III. COMPARATIVE ANALYSIS

Table 1 shows the comparative analysis of power optimization and high performance of the circuit. In this we have calculate the power of our multiplier using feed through logic and figure 7 shows the graphical representations of the average power and maximum power obtaining from the different type of multipliers circuit.

TABLE 1: EVALUATION OF POWER FROM DIFFERENT MULTIPLIER USING FEED THROUGH LOGIC

Multiplier	Average power(µW)	Max Power(µW)	Min Power(µW)
2-bit	1057.616	14820.33	464.4665
4-bit	1413.539	67198.14	55.35197
8-bit	2859.549	259471.5	275.3727

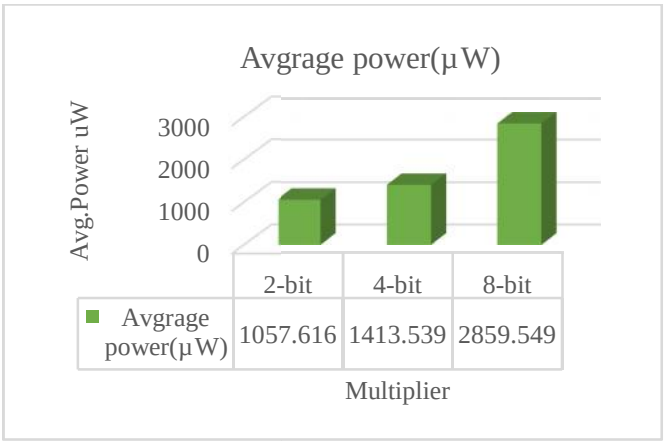


Figure 7: Average power optimizations

IV. EXPERIMENTAL RESULTS

After the simulation is carried out the following table shows the results comparison of the multiplier circuit. Table 2 show the comparison of multiplier using feed through logic which is obtained after simulation. In this we obtained the area of transistor, power optimization technology and technology library is takes place.

TABLE 2: PERFORMANCE COMPARISON

Multiplier	Technology	Techno-logy library	Supply voltage	Pavg (µW)	Area of circuit(no of transistor)
2-bit multiplier[10]	0.18 µm	UMC	1.8V	111.25	84
Proposed 2-bit multiplier with FTL	0.25 µm	Generic	1.8V	1057.616	228
Proposed 4bit multiplier with FTL	0.25 µm	Generic	1.8V	1413.539	700
Proposed 8bit multiplier with FTL	0.25 µm	Generic	1.8V	2859.549	3160

5. CONCLUSION

In this paper, we present a low power and high speed dynamic circuit. The proposed circuit is simulated in 250nm CMOS process technology using Tanner EDA 15.0 tool with Generic library file. In this work, we design the different type of multiplier with the help of new technique i.e. feed through logic. The proposed multiplier design is that we design is giving less power and efficient energy. In this dissertation we design different type of multiplier i.e. 2-bit, 4-bit and 8-bit multiplier

using feed through logic and obtaining the average power maximum power and minimum power that required to this multiplier. High speed digital circuits FTL gives advantage of having small power consumption compared to any other logic families in literature. This paper presented a Modified FTL based on partial evaluation concept. As the comparison table given is shown that FTL the 2-bit, 4-bit, 8-bit multiplier are 30%, 25% and 45% power are consumed and more efficient. The results confirmed that the multiplier using feed through logic is more efficient and low power consuming CMOS design. According to the result in tables, Modified FTL is suitable for high speed arithmetic, pipelining and filter circuit design over FTL.

Applications-

1. Increased the speed of microprocessors and different DSP processors.
2. Proposed logic will helps in designing. Low power and high speed and efficient energy for the multiplication.

REFERENCES

[1] J.M. Rabaey, A. Chandrakasan, B. Nikolic, 'Digital Integrated Circuits: A Design perspective' 2e Prentice-Hall, Upper saddle River, NJ, 2002.

[2] S. M. Kang, Y. Leblebici, 'CMOS Digital Integrated Circuits: Analysis & Design', TATA McGraw- Hill Publication, 3e, 2003.

[3] N. Weste, K. Eshraghian, 'Principles of CMOS VLSI Design, A systems perspective', Addision Wesley MA, 1988.

[4] A novel variation-aware low-power keeper architecture for wide fan-in dynamic gates. Dadgour, H.F., Joshi, R.V.; Banerjee, K.Design Automation Conference, 2006 43rd ACM/IEEE, 2006.

[5] V. Navarro-Botello, J. A. Montiel-Nelson, and S. Nooshabadi, "Analysis of high performance fast feedthrough logic families in CMOS," IEEE Trans. Cir. & syst. II, vol. 54, no. 6, Jun. 2007, pp. 489-493.

[6] Performance analysis of modified feedthrough logic for low power and high speed Sahoo, S.R.; Mahapatra, K.K. Advances in Engineering, Science and Management (ICAESM), 2012 International Conference on Publication Year: 2012R.

[7] Naveen Kumar, Manu Bansal, Navnish Kumar"VLSI Architecture of Pipelined Booth Wallace MACunit" International Journal of ComputerApplication(0975-8887)

[8] Fayed, Ayman A., Bayoumi, Magdy A., "A Merged Multiplier-Accumulator for high speed signalprocessing applications", and IEEE InternationalConference on Acoustics, Speech, and SignalProcessing (ICASSP), pp 3212 -3215, 2002.

[9] Soniya, Suresh Kumar, "A Review of Different Type of Multiplier and Multiplier-accumulator Unit", IJETTCS, 2013, vol-2, issue4.

[10] Arjun Dev,R. K. Sharma, Mayur Varshney, "A new design technique for low power dynamic feedthrough logic with delay element", Global Conference on Communication Technologies (GCCT),2015,pp197-201

[11] Sarita Singh, Sachin Mittal"VHDL Design andimplementation for optimum delay and area forMultiplier and Accumulator unit by 32 bit SequentialMultiplier" International Journal of engineeringTrends and Technology Volume3 issue 5-2012

[12] S.Shafiulla, Syed Jahangir Badashah "DesignS .Mathew, M. Anders, R. Krishnamurthy, S. Borkar, "A 4 GHz 130 nm address generation unit with 32-bit sparse-tree adder core," IEEE VLSI Circuits Symp. , Honolulu, Hi,jun2002, pp. 126-127.

[13] Salendra.Govindarajulu, Dr. T.Jayachandra Prasad, "Design of High Performance Dynamic CMOS Circuits in Deep Submicron Technology", International Journal of Engineering Science and Technology, Vol. 2(7), 2010, 2903-2917

[14] Zhiyu Liu, Volkan Kursun, "Leakage Power Characteristics of Dynamic Circuits in Nanometer CMOS Technologies", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 53, NO. 8, AUGUST 2006.

[15] Th. Haniotakis, Y. Tsiatouhas and A. Arapoyanni, "Novel Domino Logic Designs", IEEE 1999.

[16] Tyler Thorp, Gin Yee and Carl Sechen, "Domino Logic Synthesis using complex Static gates", 1998 ACM.

[17] Kumar Venkat, Liang Chen, Ichiang Lin, Piyush Mistry, Pravin Madhani, and Katsuya Sato "Timing Verification of Dynamic Circuits", IEEE 1995 Custom Integrated Circuits Conference.

[18] Themistoklis Haniotakis, Yiorgos Tsiatouhas, Dimitris Nikolos, and Constantine Efstathiou, "Testable Designs of Multiple Precharged Domino Circuits", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 15, NO. 4, APRIL 2007.