Design of Op Amp Operating in Sub threshold Region using 90nm Technology

Sreelekshmi B
Department Of Electronics Engineering
Ramrao Adik Institute Of Technology
Navi Mumbai,India
sreelekshmi@gmail.com

Mrs.Trupti Agarkar
Department Of Electronics Engineering
Ramrao Adik Institute Of Technology
Navi Mumbai,India
truptiagarkar07@gmail.com

Mrs.Sushma Kodagali
Department Of Electronics Engineering
Ramrao Adik Institute Of Technology
Navi Mumbai,India
sushmakodagali@gmail.com

***Abstract*— Op-Amps are being widely used in most of the electronic devices today varying from medical, industrial, scientific and consumer purposes. The world is now using the technology that develops more and more portable devices. The world follows the Moore's law and due to the scaling down of the transistor channel length more number of transistors can be integrated. This necessitates more battery life of the device by reducing the power consumption of each transistor. As op amps form the integral part of the circuit , by using a low power op amp can help in this power consumption of the whole device.**

The power dissipation can be made minimal either by reducing the circuit supply voltage or by bringing down the total current in the circuit or by bringing down both. Also scaling down of the devices to nanotechnology makes the low supply voltage necessary. But reducing the voltage to a very low value is not possible as the threshold voltage of the circuit will not get reduced in the same rate as that of supply voltage. So by reducing the current to the level of sub threshold current an ultra low-power op amp can be designed whose power consumption will be in the order of nano Watts.

The current in the sub threshold region of the transistors will be in the order of nano Ampere. The op amps working in sub threshold region is hence gaining attention which helps the circuit to operate under low voltage and low power. The low power op amp designed in the sub threshold region will create speed problem as the slew rate of the device will be very less due to minimum current flowing in the device. But for biomedical and sensor applications like electrocardiogram,electromyography,electroencephalography etc where the speed is not a limiting factor but the power dissipation is, there the low power op amps will be of great use.

Keywords*— *Sub threshold region, Low power Op amp, Cadence, Diffusion current

I. INTRODUCTION

The biomedical equipments like Pace maker and devices for monitoring Neuro-muscular activities etc require the sensors with low power consumption by which the battery which is implanted can work for more number of years. Whenever the gate to source potential of the transistor in the op amp is less than the sub threshold voltage, we assume that the transistor is in off state and drain to source current is zero. But exactly below the threshold the drain current is exponentially proportional to the gate to source potential. In the threshold region the inversion charge is found to be varying with the gate to source voltage exponentially. In strong inversion region the inversion charge linearly depends on gate potential. As the substrate of MOS transistor is a weakly doped region, the depletion region charge will be small. The current that flows in this region is the diffusion current. The power of the op amp is dependent on the bias current of both input and output stages. The drain current of the transistor used for biasing is the bias current.

For the transistor operating in the sub threshold region the drain current. So the power consumption of the op amp working in the weak inversion will be less than the one in saturation.

II. OP AMP IN SUB THRESHOLD REGION

The various operating region of the MOSFET are displayed in the figure 1. The MOSFET will be working in sub threshold region or weak inversion region for Vgs < Vth and Vds approximately greater than 4KT/q . The diffusion current flows in the MOSFET in the sub threshold region.

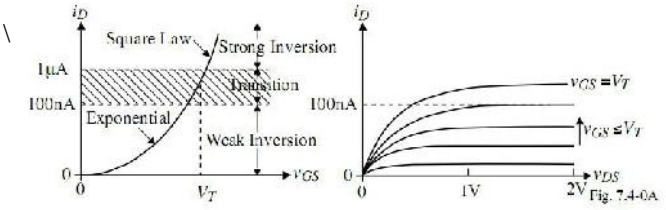


Figure 1

[1]

The expression for the sub threshold current is given by the equation:

$$I_d = I_{spec}(e^{\frac{V_{gs}-V_{th}}{nV_t}})(1-e^{\frac{-V_{ds}}{V_t}}).$$

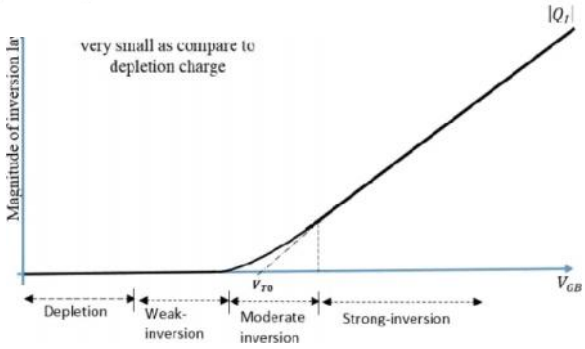
When the value of Vds > 4 (KT/q) ,the value of the expression

$$\exp^{\frac{-V_{ds}}{nV_t}} << 1.$$

So at this point the last term in expression for the drain current can be ignored,which simplifies the expression as [1]

$$I_d = I_{spec}(e^{\frac{V_{gs}-V_{th}}{nVt}})$$

where , $I_{spec} = 2n\mu \mathrm{Cox} \mathrm{Vt}^2 \frac{W}{L}$
n = Subthreshold Slope
μCox =β



From the above equation it can be interpreted that the drain current is independent on the drain source voltage and depends only on the Vgs and threshold voltage.

[1]

The transconductance can be obtained by differentiating the current equation with Vgs.

$$gm = qId/\mu KT$$

Thus the transconductance varies directly with the current and is independent of the geometry .

A. Circuit schematic

The Fig .4.4 shows the configuration of Op-amp operating in the sub threshold region. It is a two stage op amp. All the transistors used are working in the sub threshold region. NMOS pair has been made use in the input stage and PMOS current mirror forms the load. The trans-conductance of NMOS transistor is higher as compared to PMOS.Thus combination of NMOS input transistors with PMOS current mirror load provides high gain. For output stage a common source amplifiers has been used which provides higher gain as well as higher output voltage swing.

The transistors M1-M5 forms the first stage and transistors M6-M7 forms the second stage of the Op amp. Transistors M1 and M2 works as the driver transistors .These converts differential input into differential current.The current mirrored load will be converting the differential current into single ended output voltage and the transistors M3-M4 perform this function. The transistor M5 provides the bias current to the input stage.The capacitor Cc and resistor Rc forms the frequency compensation network.The frequency compensation network is necessary for achieving the closed loop stability.

- The **DC gain** of the Op amp

$$Av = gm_2\left(\frac{ro_2 ro_4}{ro_2+ro_4}\right)gm_6\left(\frac{ro_6 ro_7}{ro_6+ro_7}\right)$$

- The value of **Output resistance** is given as

$$ro = \frac{1}{\lambda I_d}$$

So,

$$Av = \frac{gm_2}{Id_2\lambda_2+Id_4\lambda_4}\frac{gm_6}{Id_6\lambda_6+Id_7\lambda_7}$$

$$\text{i.e, } Av = \frac{1}{n_2 n_6 V_t^2(\lambda_2+\lambda_4)(\lambda_6+\lambda_7)} \quad [7]$$

- **Gain-band with product**

The gain bandwidth product of the Op amp is give by

$$GBW = \frac{Id_1}{2\pi n_1 VtCc}$$

$$GBW = \frac{gm1}{2\pi Cc}$$

- **Slew rate of the Op amp**

$$SR = \frac{Id_5}{Cc} = \frac{2Id_1}{Cc}$$

$$SR = 2GBW n_1 V_t \ [7]$$

From the equations mentioned above it can be inferred that the DC gain of the sub threshold Op-amp is indepen-dent upon the drain current. It is only depend on the value of L whereas SR and GBW of the Op-amp depends on the drain current. Hence the slew rate of the Op amp will be less for an op amp working in sub threshold region [7].

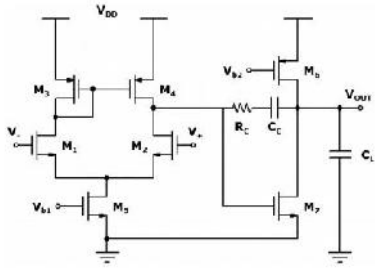


Fig 4.4 Op amp configuration
[7]

The equations are summarized in the Table 1 MOSFET parameters in sub threshold region

TABLE I
MOSFET PARAMETER IN SUB THRESHOLD REGION

Parameter	Equation
gm	Id=mV t
rd	mV t= Id

gmb	Id=mV t
n	1 + (gmb=gm)
Av0	gmrd

III. DESIGN OF THE OP AMP

The two stage op amp in the figure was designed and simulated using 90nm technology. The power supply of 1 V has been given to the circuit. The Op amp has been designed based on the specifications mentioned in the below table.Table 5.1.

TABLE II
LOW POWER OP AMP SPECIFICATIONS

Specification	Desired Value
Av(db)	>= 70
GBW	25
PM	60°
SR (V/ms)	35

These specifications are fixed in order to have DC gain and PM comparable with the previous papers and to guarantee

dynamic characteristics suitable for majority of ultra low-power system as in biomedical application.

The step by step process in setting up the design value and measuring the parameters is as below:

- At first ,the current in the MOSFET M5, to be set in below sub threshold. The Vds across the MOSFET is measured as 200mV using the DC analysis. The value is >= 4KT/q , i.e 100mV.So the simplified equation for the sub threshold current can be applied here to set the W/L value of the MOSFET.

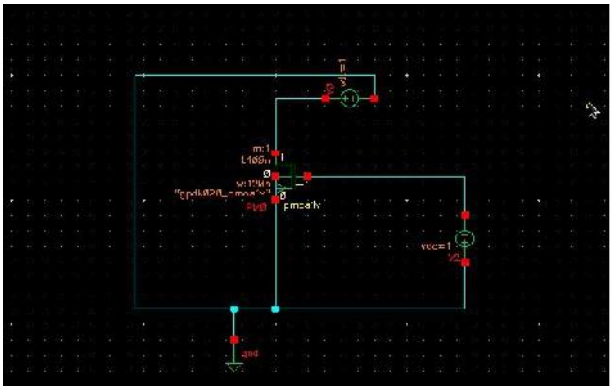


Fig. 1. PMOS Circuit V-I characteristics

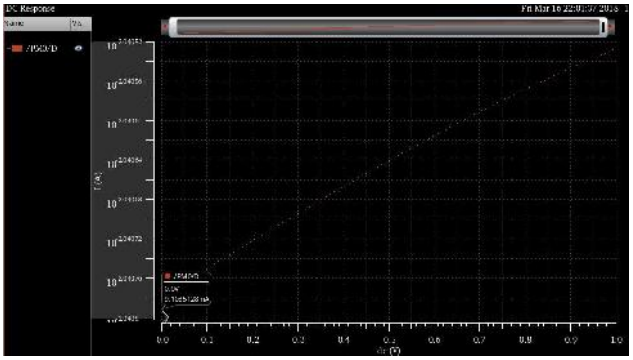


Fig. 2. Id Vs Vgs plotted for PMOS

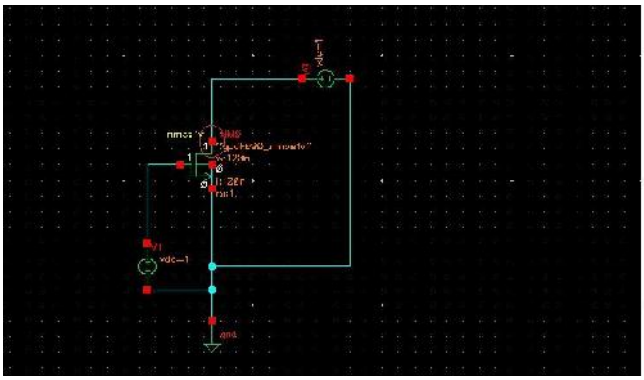


Fig. 3. NMOS Circuit V-I characteristics

- The Vth is obtained from the MOSFET specification as 200.959mV. So a gate source voltage of 150mV, which is below the sub threshold voltage is applied to the MOSFET ,M5.
- The Vth, beta and n values are obtained from the specifications details of the op amp and are substituted in the equation to get the W/L of M5.

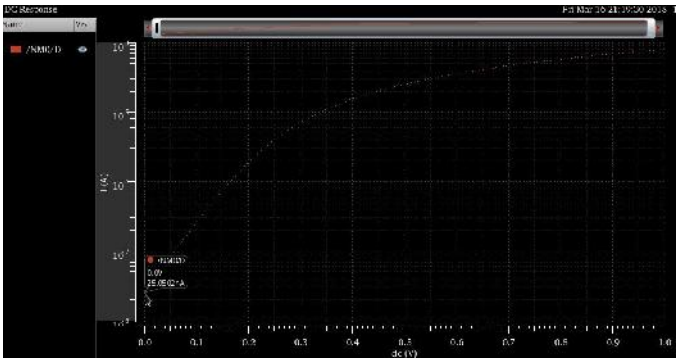


Fig. 4. Id Vs Vgs plotted for NMOS

- By setting the length of the MOSFET at least five times greater than the min L specified,the short channel effect can be eliminated. So by setting the value of L, the value of W can be calculated.
- After setting the current in M5 ,the current flowing through the MOSFET M1, M2 will be measured. This is found to be half the value of the current flowing through M5.
- The threshold voltage of the MOSFETS M1 and M2 as obtained from the specifications is found to be 201.4mV and 194.48mV respectively. So the gate voltage supply of 150 mV is applied to the M1, M2 to drive both MOSFET in below sub threshold region.
- The coupling capacitor value can be set by taking the GBW product into consideration. Using the equation

$\left(\frac{gm1}{2\pi GBW}\right)$

- The load capacitance is set as Cc/0.22
- By measuring the current through M6,M7 and deriving the W/L ration of the M6 and M7.
- The value of the M7 can be obtained from the values of I5,W 5=L5 and I7.

In order to verify that all the design criteria has been met,the two stage op amp as per the topology discussed in the previous section has been implemented. The figure below shows the circuit schematic after the implementation.

The circuit has been simulated by fixing the aspect ratio as obtained from the previous section and the circuit has been simulated and the aspect ratio,Cc,Cl values have been modified accordingly in order to obtain the best possible result as per the specifications under consideration.

The aspect ratio of the various transistors and the capacitance values are summarized and given in the below table.

TABLE III

ASPECT RATIO OF THE TRANSISTORS

MOS transistor	Designed Aspect Ratio	Actual Aspect Ratio
M1	0.66	0.8 (400/500)
M2	0.63	1 (500/500)
M5	0.43	10(5u/500n)
M7	0.75	0.6(300/500)

III. SIMULATION RESULT

The V-I characteristics of single PMOS(Fig 1 and Fig 2) and NMOS(Fig 3 and Fig 4.) has been simulated after setting up the circuit as below.

It can be seen that even at Vgs = 0 ,there is slight current in the range of nA (in NMOS) and mA (in PMOS)flowing in the circuit.

The 90nm CMOS has been used for the simulation. The sub threshold operation amplifier in
Figure 5 has been simulated using Cadence Analog Design Environment. 400m V power supply is used for biasing the Op-amp. 400pf Capacitor is used as the load at the output.

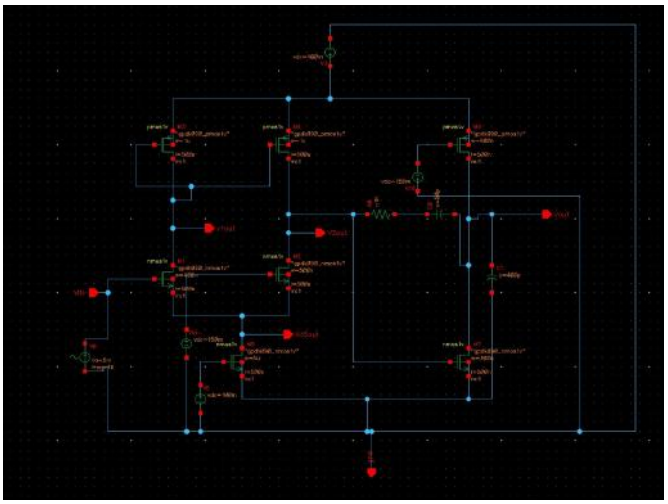


Fig. 5. Layout of the sub threshold op amp in Cadence

A.AC Analysis

AC supply of amplitude 5mV and frequency 1k Hz has been applied to the input .The frequency response of the Op amp is displayed in Figure 8. The result shows a voltage gain of 60 dB and phase margin of 80°.

The gain margin and phase margin are interpreted as from the bode plot mentioned in Fig 7.

From Fig 8 ,it can be seen that at 0 dB the frequency is 26KHz .Corresponding to this frequency the phase is 90°. So the phase margin is obtained as 180-90 = 90°. The DC gain of the Op amp is 25dB and the gain margin is 30dB.

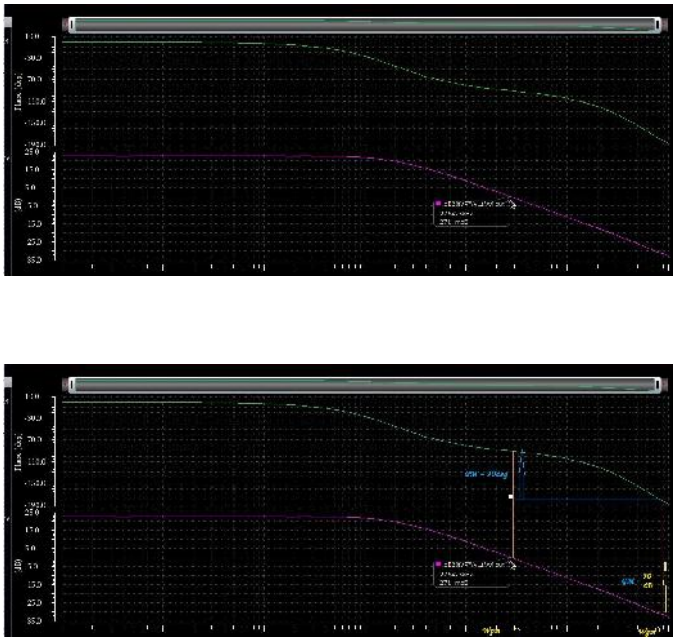


Fig. 6. AC Analysis of the subthreshold Op amp.

B. Transient Analysis

The transient analysis help us to determine the power consumption . After the simulation the below response will be obtained.

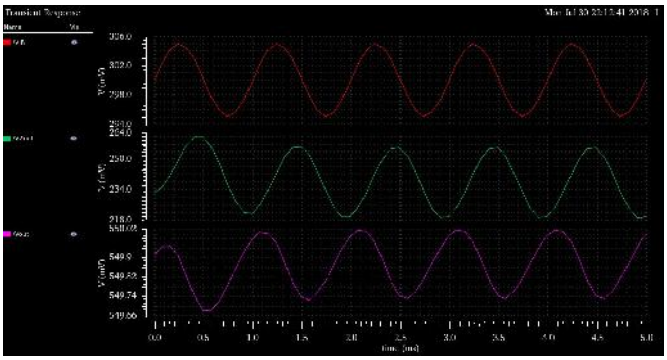


Fig 7 : Transient Response of the subthreshold Op amp.

From the curve it can be seen that the output voltage has got amplified .

C.DC Analysis

The DC analysis has been carried out in order to find the DC current flowing in the circuit . From the plot of the dc current it can be found that the current flowing in the op amp is in the nano ampere range and the current is the subthreshold current .

From the plot it can be seen that the current flowing through the MOSFET M5 is 88.84nA and the current flowing through M1 and M2 are 43.3nA and 45.54 nA respectively. From the DC operating point the current flowing through the transistor M7 is obtained as 9.44 nA.

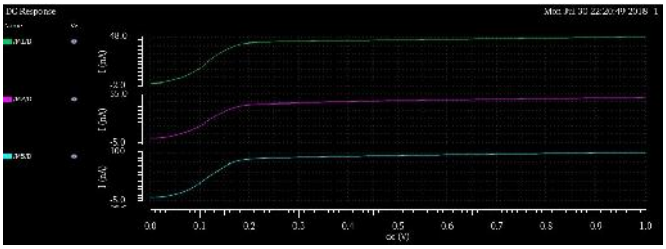


Fig 8 : DC Analysis of the subthreshold Op amp

TABLE IV
MOSFET SPECIFICATIONS

MOSFET	Beta(u)	Id(nA)	Vgs(mV)	Vth(mV)
M1	254.423	43.3	130.629	188.023
M2	319.984	45.54	130.629	191.653
M5	811.69	88.84	100	200.959
M7	188.84	9.44	83.04	182.81

D.Power Consumption:

The power curve can be plotted during the transient analysis in Cadence.The power plotted is as below :

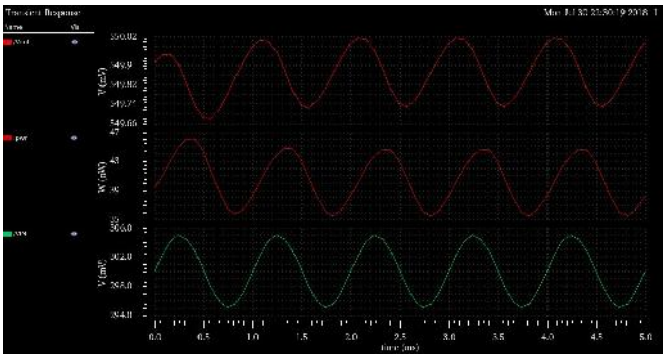


Fig 9 : Power curve of the subthreshold Op amp

From the curve we can see that the power consumption is very less which is in the nano watt range of 44.76nW which is really a very good power consumption figure for the op amp especially for the ones which is used in the bio sensor applications.

The simulated result is summarized as below:Table V

TABLE V
SIMULATION RESULTS

Parameter	Simulated result
Supply Voltage	400m V
Id (M1)	43.3 nA
Id (M2)	45.54nA
Id (M3)	43.41nA
Id (M4)	43.23nA
Id (M5)	88.84nA
Id (M6)	9.44nA
Id (M7)	9.44nA
Power Consumption	44.76 nW
DC gain	24dB
Unity gain BW	26KHz
Phase Margin	90 degree
Process	90nm

IV. LAYOUT OF THE SUBTHRESHOLD OP AMP.

Layout of a circuit is the representation of the circuit in terms of planar geometric shapes. This shapes represents the patterns of metal,oxide or semiconductor layer that make up the component of the circuit. The position and the connection between the geometric shapes controls the behaviour of the final circuit.

Once the layout is generated,it must undergo a series of checks and the process is called physical verification.The various physical verifications are

1.Design Rule Checking
2.Layout Versus Schematic
3.Parasitic Extraction.

A.Design Rule Checking

Design rule checking is the major step during the physical verification of the circuit. It basically checks whether the physical layout of the circuit meets a set of parameters called design rules. The design rule set implies the connectivity and geometric restriction to ensure that the parts of the circuit work properly.

Some examples of DRC in design are :

- Minimum channel length of the transistor
- Minimum metal width
- Metal to metal spacing
- Poly density

B.Layout Versus Schematic

LVS is a class of electronic design automation that verifies whether the circuit layout corresponds to the original schematic . The LVS checking software recognizes the drawn shape of the layout that represents the electronic components as well as the connection between them. The LVS check will compare the schematic netlist with the layout netlist.

The typical errors which are detected are

- Shorts
- Opens
- Component Mismatch(Component of incorrect type used)
- Missing component
- Parameter mismatch (match upto the tolerance as allowed by the LVS tool)

C.Parasitic Capacitance Extraction

Parasitic capacitance or stray capacitance is an unavoidable capacitance that exists between the parts of an electronic circuit because of the proximity to each other. When there are two conductors which are close to each other and at different potential ,the electric field between them causes the electric charge to be stored between them which will give rise to parasitic capacitance.

Parasitic extraction is the technique by which the parasitic capacitance can be calculated using the EDA tools and this can be included in the circuit simulation.

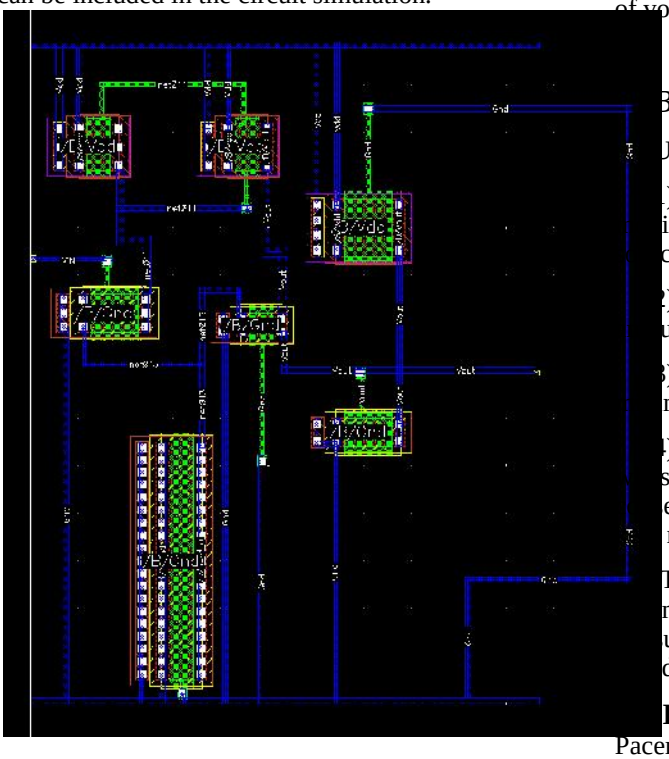


Fig 10 .Layout of the subthreshold Op Amp

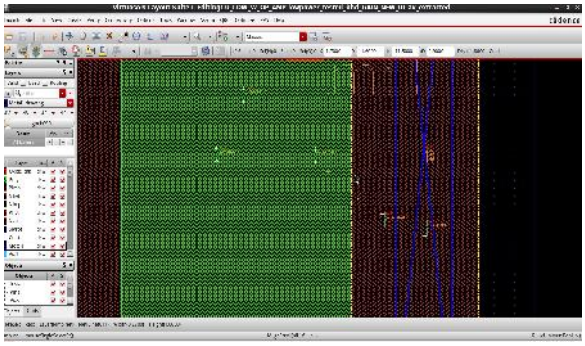


Fig 11.Parasitic Capacitance Extraction

V.ADVANTAGE,DISADVANTAGES AND APPLICATIONS ,OF LOW POWER OP AMPS IN SUB THRESHOLD REGION

Ultra low power op amps are having the following advantages and disadvantages

A. Advantages and Disadvantages

Advantages:

High gain and low power are the major advantages of the op amp operating in sub threshold region. So this finds application in the low-voltage / low-power applications that might be powered e.g. by energy harvesting, where supply voltages have to be as low as possible to avoid additional losses.

Disadvantages:

The op amp working in sub threshold region is having increased propagation delay,poor slew rate and increased variation in device to device due to exponential dependency of voltage/current.

B. Applications:

Ultra low power electronics finds applications in below:

1) Battery operate systems which are portable and ile. More portable the system smaller will be the energy ce and stringent will be the power constraint.

2) Systems that operate by harvesting relatively small unts of energy from their environment.

3) Systems in which the heat dissipation needs to be mized.

4) Complex systems which consists of many devices se complexity simply will not scale unless the power and equently heat dissipation of each of their compo-nents is minimal.

The low power op amps working in sub threshold region mainly used for the applications in which the power umption is a major factor of concern and not the d.Hence it finds useful in biomedical applications [3].

Electronic biomedical system

Pacemaker, hearing aid, Neural recording, retinal stimulator, body-area monitoring etc are a few biomedical systems that works on low power. The biomedical devices that are

implanted in the body must be small with low heat dissipation . Also as in pacemakers the device must be driven by a non rechargeable battery which will be having a battery life of many years. A fully implanted system operated by a rechargeable battery must be utilizing very low power so that the system can work up to 20-30 years without the need of battery replacement[3].

VI.CONCLUSION

In this paper the design of the two stage low power op using 90nm technology has been presented. The circuit has been designed,implemented and simulated using the professional software of Cadence. This Op amp is having 24dB gain,90degree Phase Margin and the power consumption is only 253nW. The low power consumption makes it truly ideal for the biomedical systems such as cardiac pacemaker, Electrocar-diogram etc. where the low power consumption is the major criteria and the requirement of high bandwidth and slew rate is not a major concern.

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