Review: Optimization Techniques for Multirate Digital Filters

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Abstract— **Multirate filtering technique is widely used for meeting the sampling rates of different subsystems connected in cascade. Realization of Multirate system is cheaper than single rate system. But still it has huge scope to optimize the Multirate filters. This paper reviews different approaches for optimizing Multirate digital filter based on various optimization techniques such as Pipelining, Parallel processing, Retiming, Unfolding, Folding, Systolic architectural design. These optimization techniques provide the satisfactory frequency response with less power consumption, less area and more speed. Multistage implementation reduces the computational load to a large extent.**

Keywords: **Multirate filters, Multistage filters, Retiming, Pipelining, Parallel processing, Unfolding.**

I. INTRODUCTION

Multirate signal processing is widely used in the areas like communications systems, audio systems, medical electronics, multimedia systems etc. The main operations in Multirate DSP are Decimation and Interpolation. Decimation reduces the sampling rate while interpolation increases the sampling rate by an integer number. The sampling rate can also be changed by a fractional number. In case of decimation, filtering is required to suppress aliasing and then reducing the sampling rate. While in case of interpolation the sampling rate is increased first and then filtering is used to remove images. The filter is to be designed appropriately so that altering the sampling rate does not destroy the desired signal component significantly.

The importance of Multirate filtering is two-fold in modern digital signal processing. Firstly there are several instances when there is a need to change the sampling frequency of a digital signal. The main reason for re-sampling is a need to pass data between two systems that use incompatible sampling rates [1]. These filters can achieve both greatly reduced filter lengths and computational rates as compared to standard single-rate filter designs and thereby provide a practical solution to an otherwise difficult problem. Secondly multirate filtering is used in constructing the filter banks.

Direct form realization of such filters is costly and involves more computations [1][2]. There are various optimization techniques such as Retiming, Parallel processing, Pipelining, Folding, Unfolding which may be used for optimizing filter parameters [2][3]. These techniques can be used to optimize the filters in terms of power, area and speed. The Multirate multistage filters provide more computationally effective structures.

II. LITERATURE REVIEW

N. Onwuchekwa et al. proposed the efficient approach of Multirate signal processing which reduces the number of filter operations as well as the memory requirements by a decimation factor M and interpolation factor L. Power consumption is reduced by polyphase decomposition [2].

M. Madheswaran et al. briefed about the CIC Filter with various filter structures and their implementations on Field Programmable Gate Array (FPGA) board. The performance of multiplier less filter is analyzed in terms of power consumption [3].

Xue-Yang Zhu et al. proposed new methods for finding a feasible retiming and an optimal retiming so that a Signal Data Flow Graph (SDFG) achieves its smallest iteration period. Both methods work directly on the SDFG without converting it to its equivalent Homogeneous Synchronous Data Flow Graph HSDFG. This reduces the execution time [4].

Xue-Yang Zhu et al. presented an exact method and a heuristic method for static rate-optimal scheduling of SDFGs using explicit retiming and implicit unfolding. Fixed random order of firings is used to generate a constrained self timed execution STE in the heuristic method [5].

Xue-Yang Zhu examined the relationship between SDFG and its equivalent HSDFG, and proved some useful properties by which iteration period can be computed directly on SDFGs. Based on the efficient algorithm for computing iteration period, a retiming algorithm for reducing iteration period of SDFGs has been provided. It has reduced the iteration period of an application to meet the real time requirements [7].

Ying Yi,MarkMilward et al. presented a synthesis methodology based on Modular Design Procedure (MDP) [2][3] which provides a bridge between the high-level algorithm, architecture mapping techniques and lower level design tools when targeting multirate DSP. Timing related problems associated with the implementation of the Multirate DSP algorithm are addressed properly [8].

III. MULTIRATE FILTERING TECHNIQUES

In Multirate filtering, FIR (Finite Impulse Response) or IIR (Infinite Impulse Response) filter can be used. An FIR filter easily achieves a linear phase response but requires a larger number of operations per output sample when compared with an equal magnitude response of IIR filter. Multirate techniques

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significantly improve the efficiency of FIR filters that makes them very desirable in practice [1].

Fundamental operations in Multirate signal processing are decimation and interpolation. Multirate signal processing alters the sampling without significant error in the output [1] [2]. In decimation, the sampling rate is reduced from Fs to Fs/M by discarding $M - 1$ samples for every M samples in the original sequence.It consist of digital antialising filter h(k) and a sample rate compressor, symbolized by down arrow and the decimation factor 'M' as shown in fig 1(a).

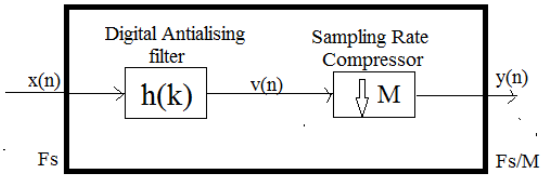

Fig 1(a) Decimator

Interpolation is the exact opposite of decimation. Interpolation inserts L-1 samples in between two consecutive samples of original signal. Anti imaging filter is to be placed after expander as shown in fig 1(b). Therefore the sampling rate increases from Fs to L.Fs[2].

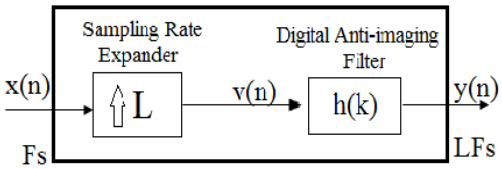

Fig.1 (b) Interpolator

Rational Sampling Rate Conversion is nothing but changing the sampling rate by a ratio of two integers i.e. L/M. It can be performed by cascading an interpolator followed by a decimator [3][2].

The polyphase structure is obtained when an N^{th} order filter transfer function is decomposed into M /L polyphase components constrained to M/L<N. Due to polyphase Multirate implementation, the number of arithmetic operations in a linear phase FIR filter is decreased by a factor M (or L). An effective method, which leads to high efficiency for a high-order FIR filter is proposed in [6]. For multirate IIR filters, several approaches to polyphase decomposition have been developed in [6] and [16]. For a rational conversion factor L/M, an efficient decomposition of the N^{th} order IIR filter based on the method given in [6] is proposed in [11]. The efficiency of FIR filters for sampling rate conversion is significantly improved using the polyphase realization.

IV. VLSI-DSP Optimization Techniques

Optimization is a procedure used in the design of a system to maximize or minimize some performance index. The possible performance indices of a Multirate DSP are speed of execution, memory usage (code size and data size) and power consumption. In Multirate DSP there are various VLSI-DSP techniques such as Retiming, Parallel processing, Pipelining, Folding, Unfolding available to optimize digital filter [5][6].

Retiming is a transformation technique used to change the location of delay elements in a circuit without affecting the input -output characteristics of the circuit. It reduces the critical path of the system as shown in fig 2(a). Pipelining can be viewed as a special case of Retiming. Parallel Processing replicates the system as shown in fig 2(b) and processes the samples simultaneously thereby increasing the speed of operation. In Parallel processing multiple outputs are computed in parallel and effective sampling speed is increased by the level of parallelism. Pipelining and Parallel Processing also lead to a reduction in the critical path as well as in the power consumption [7] [6].

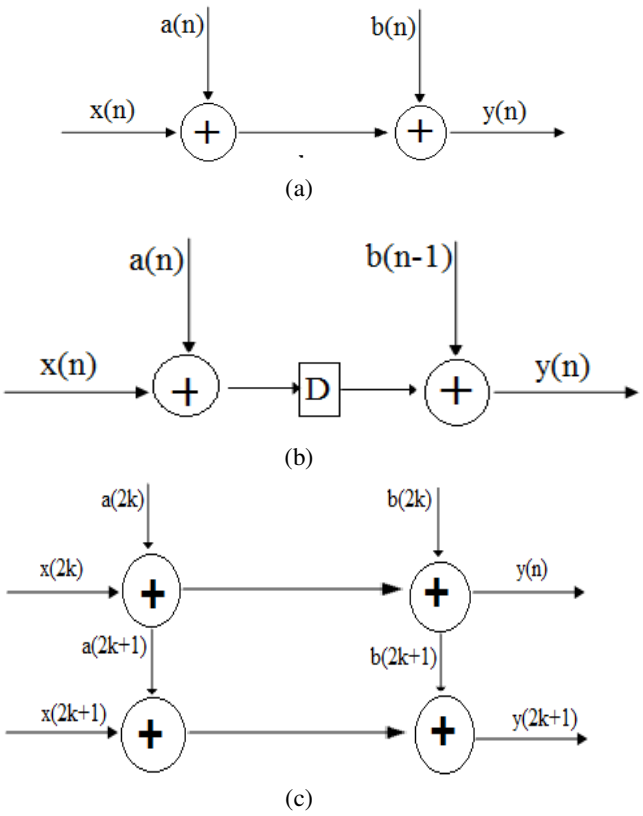

Figure2 (a): A data path (b): The 2-level pipelined structure of (a)(c): The 2-level parallel processing structure of (a)

Unfolding is a transformation technique that can be applied to a DSP program to create a new program describing only one iteration of the original program. Unfolding is also referred as loop unrolling and has been used in compiler theory. It has application in designing high speed and low power VLSI Architectures and also in designing the parallel architecture at word level and bit level [7][8].

DSP application is extremely computationally demanding, but often requires low power, low memory use. Modern

processor use increased parallelism to get high performance on DSP tasks. It has many applications in synchronous design. These applications include reducing clock period of the circuit, reducing the numberof register in circuit, reducing the power consumption of the circuit and logic synthesis.

V. MULTIRATE DESIGN METHODOLOGIES

Low power and high speed are the two most important features for many signal processing system designs. Particularly in real time multimedia applications, there are many approaches to achieve high speed and low power at different levels. The complexity of the resulting realization depends on the size, numbers, and typeof multiplication, adder and delay blocks [9][10]. These filters can achieve reduced filter lengths and higher computational rates as compared to single-rate filter designs. These filters are of an essential importance in communications, image processing, digital audio and multimedia applications. Multistage and polyphase are the two methodologies which can be used for reducing the computational requirements, enhancement of speed and reducing power consumption.

When large changes in the sampling rate are required, it is more efficient to change the rate in two or more stages. In fact, most practical multirate systems employ the multistage approach because it allows a gradual reduction or increase in the sampling rate, leading to a significant relaxation in the requirement of the anti-aliasing or anti-imaging filter at each stage and computational requirements [8].

Fig 3 shows an I-stage decimation process. The overall decimation factor M is expressed as the product of smaller decimation factors which must be positive integers.

$$M = M_1 M_2 \ldots\ldots\ldots M_I$$

Each stage is an independent decimator as shown in Fig 3.

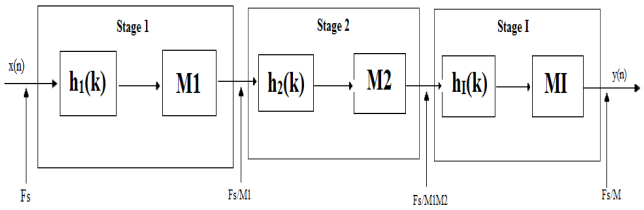

Fig. 3 Multistage decimation process

The design of practical multistage sampling rate converter can be broken down into four steps:

1. Specify the overall anti aliasing or anti imaging filter requirements.
2. Determine the optimum number of stages for decimation or interpolation that will yield the most significant implementation.
3. Determine the decimation or interpolation factor for each stage.
4. Design appropriate filter at each stage.

The filter requirements for each stage of filter to avoid aliasing after rate reduction are given as follows:

Passband $0 \le f \le fp$

Stopband $(Fi\text{-}Fs/2M) < f < Fi\text{-}_1/2$, i=1, 2, 3… I

Passband Ripple ∂_p / I

Stopband Ripple ∂_s

Filter length $N \approx [D_{\infty}(\partial p, \partial_s)/\Delta f_i] - f(\partial_p, \partial_s)\Delta fi + 1$

Where,

$f_p, F_i, N, \Delta f_i$, are the passband edge frequency, output sampling frequency, the filter length and normalized transition width for the i^{th} stage decimator respectively. For multistage decimation, a lower passband deviation is necessary for each stage to ensure that the passband deviation should be ∂_p / M_i. The stopband deviation for each stage is same as the overall stopband deviation ∂_s because as signal goes from stage to stage the stopband component are attenuated further.

Determining the Number Of Stages And Decimation Factors

The multistage design offers significant saving in computation and storage requirements over a single-stage design. The extent of this saving depends on the number of the stages used and the choice of decimation factors for the individual stages. A major problem is to determine the optimum number of stages *I* and the decimation factors for each stage. An optimum number of stages are the one which leads to the least number of Multiplications per Second (MPS) and the Total Storage Requirements (TSR). MPS and TSR can be computed using the formulae given in 1 and 2.

$$MPS = \sum_{i=1}^{I} Ni.Mi \qquad 1$$

$$TSR = \sum_{i=1}^{I} N_i \qquad 2$$

Where,

Ni is the number of filter coefficients for i^{th} stage. The choice of the number of stages *I* and decimation factors is not a trivial problem. However, in practice the number of the stages *I*are rarely more than 3 or 4. Thus a viable approach is to determine all the possible factors of M, that is all the set of Mi values, and their corresponding MPS or TSR.

In general, for optimum MPS or TSR the decimation factors should satisfy the following relationship (Crochiere and Rabiner, 1975, 1976):

$$M_1 > M_2 > \ldots > M_I$$

From above discussion , it is clear that, in general, multistage designs yield very significant reduction in computation, storage requirements and power consumption as compared to single-stage designs. The limitations of this

approach are that proper control structure is required to implement the system and proper values of I should be chosen.

Another approach for optimizing the Multirate filter is polyphase decomposition. Polyphase decomposition splits a Finite Impulse Response (FIR)Multirate filter into appropriate number of subfilters.The key to the efficiency of polyphase filtering is that specific input values are only multiplied by selected values of the impulse response in the downsampled convolution. By splitting the filter coefficients into two polyphase subfilters, computations are reduced. The outputs of the subfilters are interleaved and summed to yield the filter output. There are various methods to implement the polyphase filters. The basic polyphase filter implementationis shown in fig 4(a) and its efficient implementation is shown in fig 4(b) [12][13].

During decimation, a signal is down sampled by throwing away intermediate samples which results in aliasing [11]. To prevent aliasing,an anti-aliasing lowpass filter with transfer functionH(z) is employed before downsampler as shown in fig 4(a).In this case the samples are processed and then dropped down. It can be made efficient by dropping the samples first and then process it as shown in fig 4(b).Polyphase approach greatly reduces the power consumption and area along with enhancing the speed of operation [12].

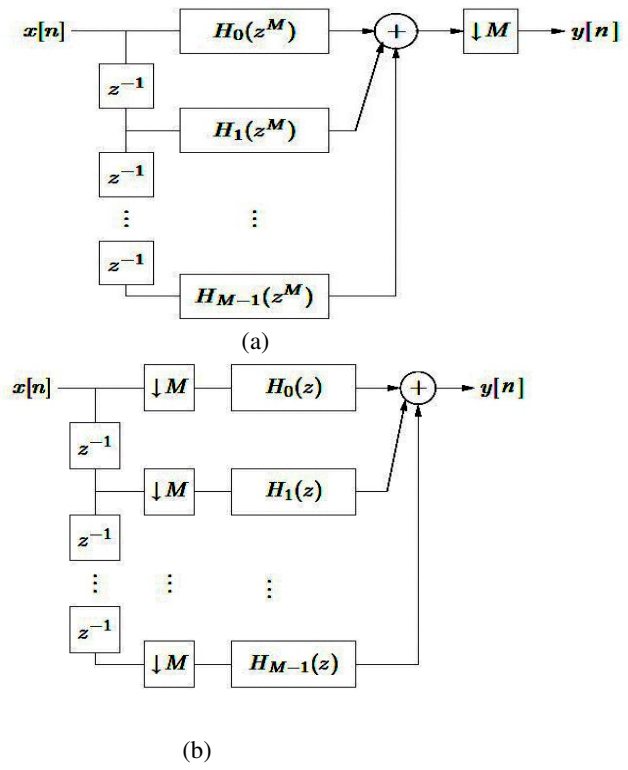

Fig 4.Polyphase implementation of FIR decimator: (a) Filter and downsampler. (b) Efficient polyphase decimator

VI. CONCLUSION

By reviewing the various papers, it can be concluded that Multirate filter can be optimized using different approaches. Pipelining and parallel implementation of Multirate filter results in low power consumption and less critical path. Multistage design approach reduces the order to realize filter drastically thereby relaxing the computational complexity. Polyphase decomposition gives higher speed of operation and less power consumption.

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